REMARKS

Reconsideration and allowance of the present application are respectfully requested. By this communication, the Abstract and claim 6 have been amended, and claim 14 has been added. Support for the subject matter added to claim 6 can be found variously throughout the Specification, for example, at lines 1-12 of page 4. Moreover, support for the subject matter recited in claim 14 can be found variously throughout the Specification, for example, at line 18 of page 3 through line 12 of page 4. Claims 6-14 are pending.

In numbered paragraph 1, on page 2 of the Office Action, the Abstract of the disclosure is objected to because of an alleged informality. In particular, the Examiner alleges that the term "Figure 4" should be deleted from the Abstract. Applicant notes however, that the Abstract provided in corresponding U.S. Patent Pub. No. 2005/0280460 does not include the "Figure 4" term. For at least this reason, Applicant believes that the requested correction is not required. However, in an effort to expedite prosecution, a new substitute Abstract is provided herewith. Accordingly, Applicant requests that the objection to the Abstract be withdrawn.

In numbered paragraph 2, on page 2 of the Office Action, the Information Disclosure Statement (IDS) filed on November 23, 2005 is alleged to not comply with 37 CFR 1.98(a)(1). As explained in the subject IDS statement, the references cited in the International Search Report provided in the IDS have been previously made of record in the application. Specifically, the Reference (U.S. 6,452,433) was submitted in an IDS filed on December 30, 2004. Thus, the reference identified in the International Search Report has been considered by the Examiner. Accordingly, Applicant submits that no further correction is necessary.

In numbered paragraph 3 on page 2 of the Office Action, claims 6-9 are rejected under 35 U.S.C. §102(b) as anticipated by *Chang et al* (U.S. Patent No. 6,452,433. Applicant respectfully traverses this rejection.

As variously exemplified in Figs. 3-5, an exemplary embodiment of the instant invention includes a latch circuit 110 that is divided into a left portion 116 and a right portion 62. The circuit 110 includes complementary clock inputs 52 and 54 and outputs 112 and 114. Further, a plurality of bipolar transistors, capacitors, resistors, current sources and transistors are provided and connected in a manner to achieve the latching function. In particular, transistors 118 and 78 are connected to form a transistor clock pair that receive complementary clock inputs 52 and 54, respectively. Transistor 118 has a larger emitter area than transistor 76, thus making the transistor clock pair "imbalanced" in having a "hold period/follow period" ratio that is greater than 1.

The foregoing features are broadly encompassed by claim 6, which recites that the first and second clock transistors form a transistor clock pair and each of the clock transistors receive complementary inputs to define a "hold period/follow period" ratio for the transistor clock pair, where the emitter area of the first clock transistor is greater than that of the second clock transistor such that the "hold period/follow period" ratio of the transistor clock pair is greater than 1.

The *Chang* patent discloses a latch circuit 1100 that includes a differential transistor pair having a first transistor 1112 and a second transistor 1114. The first transistor 1112 has an emitter area A1 and a second transistor 1114 has an emitter area A2 that is greater than A1. A master clock signal 1104 and a first transistor 1112 are associated with a sample period, and the master clock signal 1106 and a

second transistor 1114 are associated with the hold period. In other words, the *Chang* patent teaches that the first transistor 1112 is associated with the master latch and the second transistor 1114 is associated with the slave latch. Based on this configuration, it is readily apparent that the emitter area A2 of the second transistor 1114, which is in the slave latch is greater than the emitter area A1 of the first transistor 1112, which is in the master latch.

In contrast, claim 6 recites that the emitter area of the first clock transistor is greater than that of the second clock transistor such that the hold period/follow period ratio of the transistor clock pair is greater than 1. As shown, for example, in Fig. 4 of the drawings the first transistor 118 is associated with the master latch and the second transistor 78 is associated with the slave latch. This configuration is far different from the teachings of the *Chang* patent. Furthermore, *Chang* does not teach or suggest that a transistor in the master latch can have a larger emitter area than a transistor in the slave latch. For at least this reason, claim 6 is not anticipated by the *Chang* patent.

To properly anticipate a claim, the document must disclose, explicitly or implicitly, each and every feature recited in the claim. *See* Verdegall Bros. v. Union Oil Co. of Calif., 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987. *Chang* fails to disclose, teach, or suggest every element recited in independent claims 1, 11, and 12, therefore these claims are not anticipated by *Chang*. Accordingly, Applicant respectfully requests that the rejection of claim 6 under 35 U.S.C. §102 be withdrawn, and this claim be allowed.

In numbered paragraph 5 on page 3 of the Office Action, claims 6-9 are rejected under 35 U.S.C. §102(b) as anticipated by *Muller* (U.S. Patent No. 4,289,979). Applicant respectively traverses this rejection.

The *Muller* patent discloses a D-type flip-flop having a clock signal that switches on the multi-emitter transistors T7 and T14. These multi-emitter transistors have an emitter size that is approximately three times the size of the other transistors used in the flip-flop. As shown in Fig. 1, however, the master latch portion 15 and the slave latch portion 17 each have its own respective transistor clock pairs that include transistor T7 and T14, respectively. In fact, there is no transistor clock pair that is configured to be shared by the master flip-flop 15 and the slave flip-flop 17. For at least this reason, the configuration as recited in claim 6 is not anticipated by the *Muller* patent. In particular, the *Muller* patent fails to teach or suggest a first latch portion that includes a first clock transistor, a second latch portion that includes a second clock transistor, and that the first and second clock transistors form a transistor clock pair as recited in claim 6. Accordingly, Applicant request that the rejection of claim 6 under 35 U.S.C. §102(b) be withdrawn, and this claim be allowed.

Claims 7-9 depend from claim 6. By virtue of this dependency, Applicant submits that these claims are allowable for at least the same reasons given above with respect to claim 6. In addition, Applicant submits that these claims are further distinguishable over the *Chang* patent and the *Muller* patent by the additional elements recited therein. Applicant requests, therefore, that the rejection of claims 6-9 under 35 U.S.C. §102 be withdrawn, and these claims be allowed.

In numbered paragraphs 8 and 9 of the Office Action, claims 10-13 are rejected under 35 U.S.C. §103(a) as being unpatentable over the *Chang* patent and the *Muller* patent, respectively. Because claims 10-13 depend from claim 6, and the *Chang* patent and the *Muller* patent fail to disclose each and every element recited in claim 6, Applicant submits that claims 10-13 are allowable by virtue of their dependency. Accordingly, Applicant requests that the rejection of claims 10-13 under 35 U.S.C. §103 be withdrawn and these claims be allowed.

In numbered paragraph 10 on page 5 of the Office Action, claims 10-13 are rejected under 35 U.S.C. §103(a) as unpatentable over *Denny* (U.S. Patent No. 4,922,127). Applicant respectfully traverses this rejection.

The *Denny* patent discloses a phrase shift circuit having a plurality of transistors arranged in a master/slave flip-flop switching arrangement. Two of these transistors, T_{14} and T_{15} are described as having a different emitter area than the other transistors. As shown in Fig. 5, transistors T_{14} and T_{15} are formed in a transistor pair arrangement. The *Denny* patent however, does not describe the size relationship between transistors T_{14} and T_{15}, but only indicates that the sizes of these transistors are different from the other transistors provided in the circuit arrangement. For at least this reason, the *Denny* patent fails to teach or suggest a transistor clock pair as recited in claim 6, and thus, by virtue of their dependency, fails to teach or suggest the additional elements recited in claims 10-13.

To establish *prima facie* obviousness of a claimed invention, all of the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). Moreover, obviousness "cannot be established by combining the teachings of the prior art to produce the claimed invention, absent

some teaching or suggestion supporting the combination." ACS Hosp. Sys. V. Montefiore Hosp., 732 F.2d 1572, 1577, 221 USPQ 929, 933 (Fed. Cir. 1984). For at least the above reasons, Applicant respectfully requests that the rejection of claims 10-13 under 35 U.S.C. §103 be withdrawn, and these claims be allowed.

Newly added claim 14 depends from claim 6 and is allowable for the same reasons discussed above. Applicant requests that claim 14 be examined and allowed.

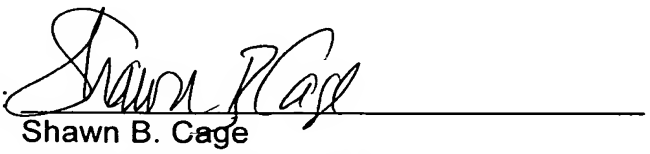
Conclusion

Based on at least the foregoing amendments and remarks, Applicant submits that claims 6-14 are allowable, and this application is in condition for allowance. Accordingly, Applicant requests a favorable examination and consideration of the instant application. In the event the instant application can be placed in even better form, Applicant requests that the undersigned attorney be contacted at the number below.

Respectfully submitted,

BUCHANAN INGERSOLL PC

Date: May 3, 2006

By: 

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